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(54) **V-SHAPED SIGE RECESS VOLUME TRIM FOR IMPROVED DEVICE PERFORMANCE AND LAYOUT DEPENDENCE**

(71) Applicant: **Taiwan Semiconductor Manufacturing Co., Ltd., Hsin-Chu (TW)**

(72) Inventors: **Chao-Hsuing Chen, Tainan (TW);**
Ling-Sung Wang, Tainan (TW);
Chi-Yen Lin, Tainan (TW)

(73) Assignee: **Taiwan Semiconductor Manufacturing Co., Ltd., Hsin-Chu (TW)**

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H01L 29/04 (2006.01)

H01L 29/08 (2006.01)

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CPC **H01L 29/66636** (2013.01); **H01L 29/045** (2013.01); **H01L 29/0847** (2013.01); **H01L 29/7848** (2013.01)

(58) **Field of Classification Search**

USPC 257/190; 438/300
See application file for complete search history.

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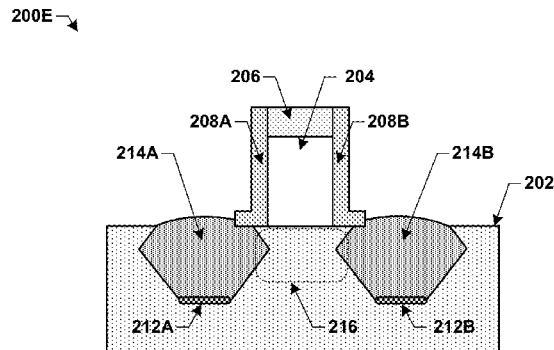
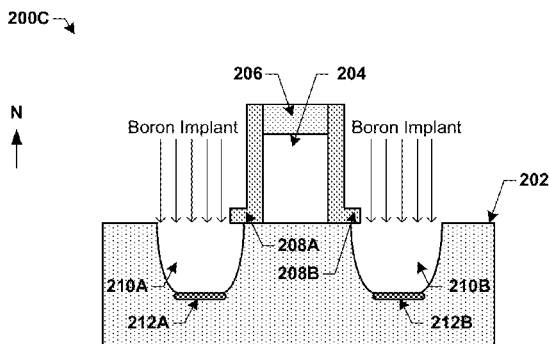
Primary Examiner — Asok K Sarkar

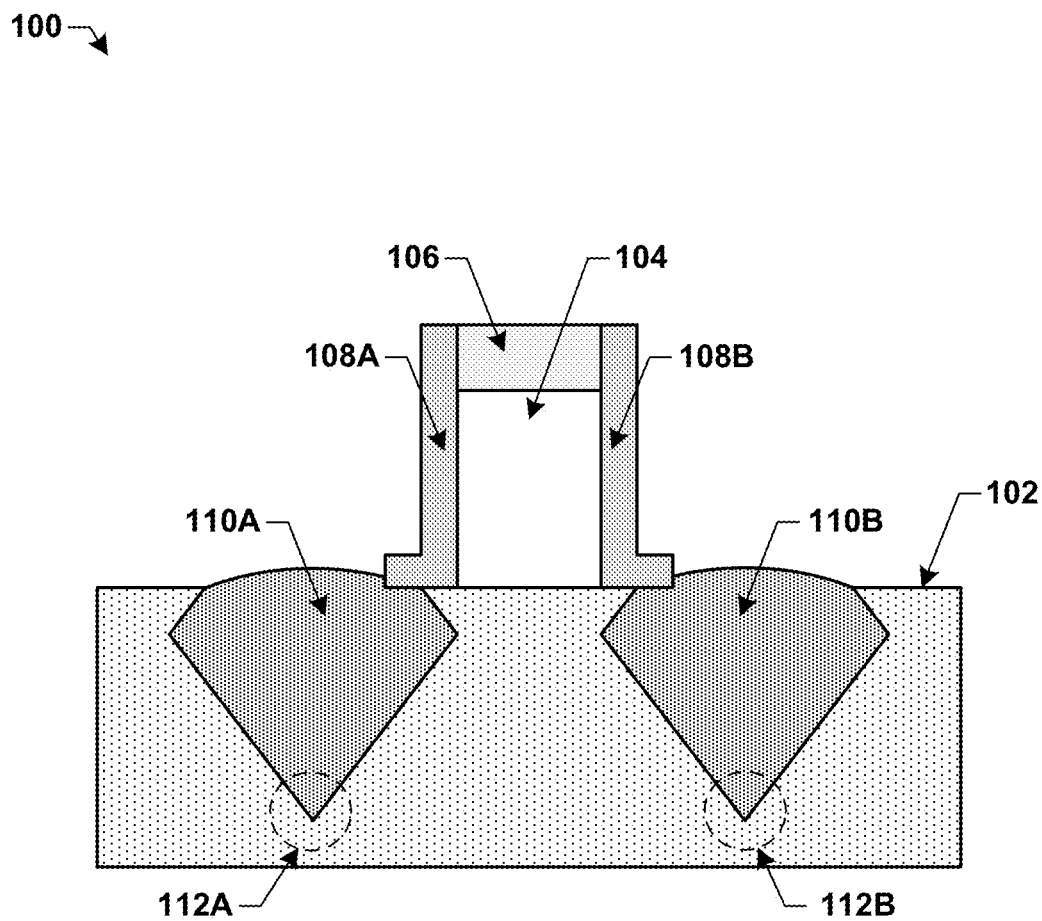
(74) *Attorney, Agent, or Firm* — Eschweiler & Associates, LLC

(57) **ABSTRACT**

Some embodiments of the present disclosure relates to a method and a device to achieve a strained channel. A volume of a source or drain recess is controlled by a performing an etch of a substrate to produce a recess. An anisotropic etch stop layer is then formed by doping a bottom surface of the recess with a boron-containing dopant, which distorts the crystalline structure of the bottom surface. An anisotropic etch of the recess is then performed. The anisotropic etch stop layer resists anisotropic etching such that the recess comprises a substantially flat bottom surface after the anisotropic etch. The source or drain recess is then filled with a stress-inducing material to produce a strained channel.

20 Claims, 5 Drawing Sheets



**Fig. 1**

200A →

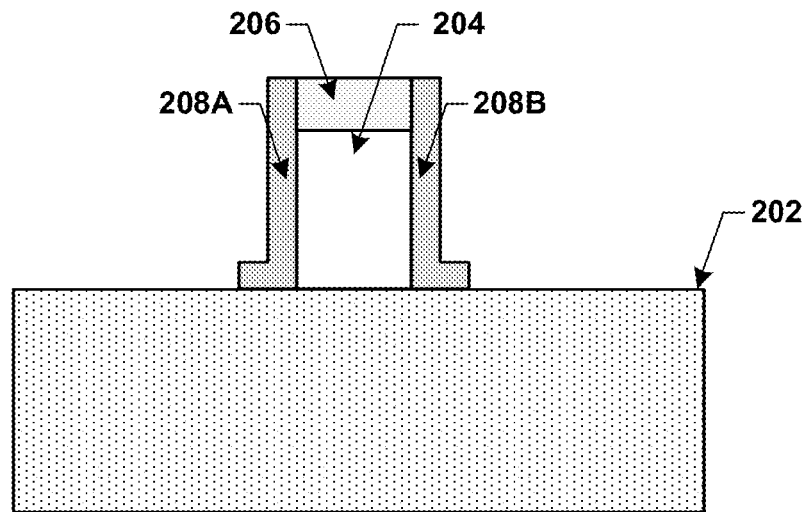


Fig. 2A

200B →

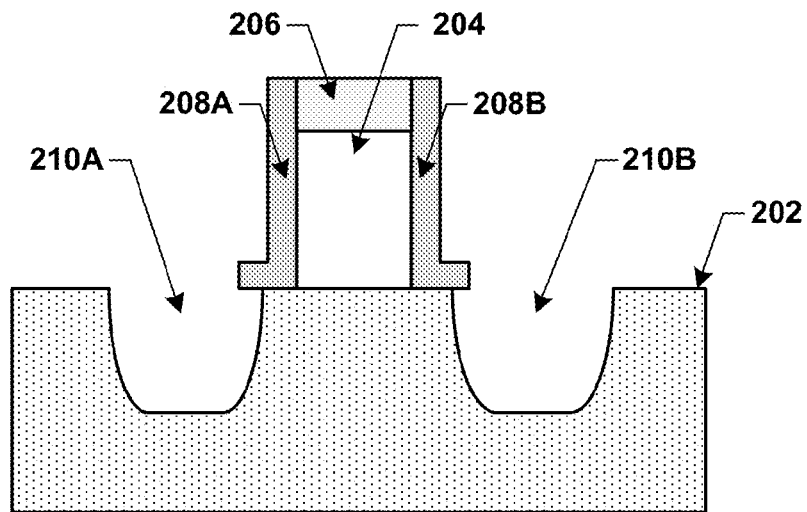


Fig. 2B

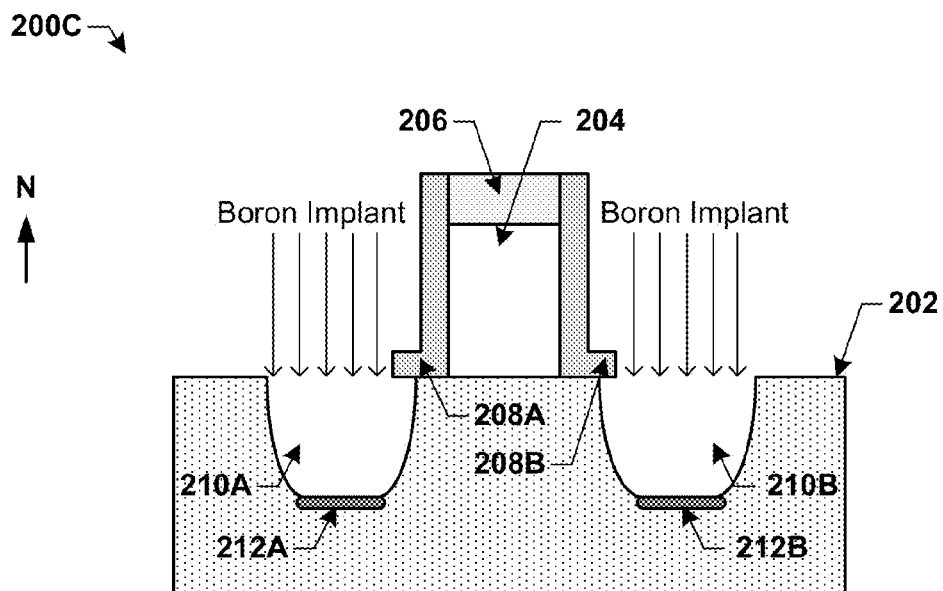


Fig. 2C

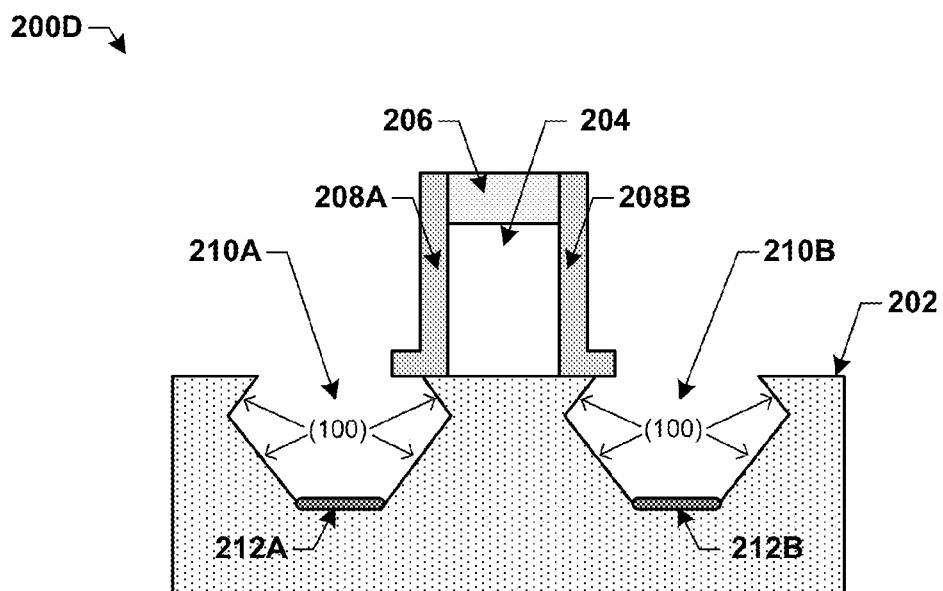


Fig. 2D

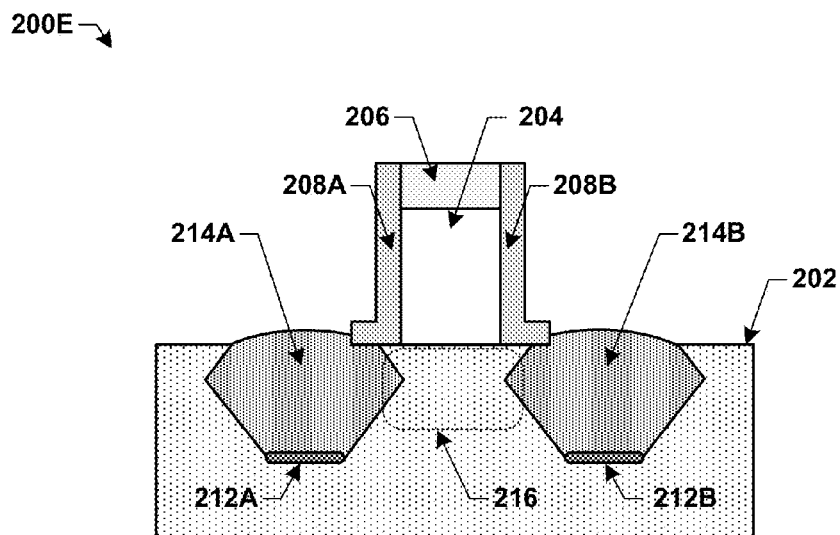


Fig. 2E

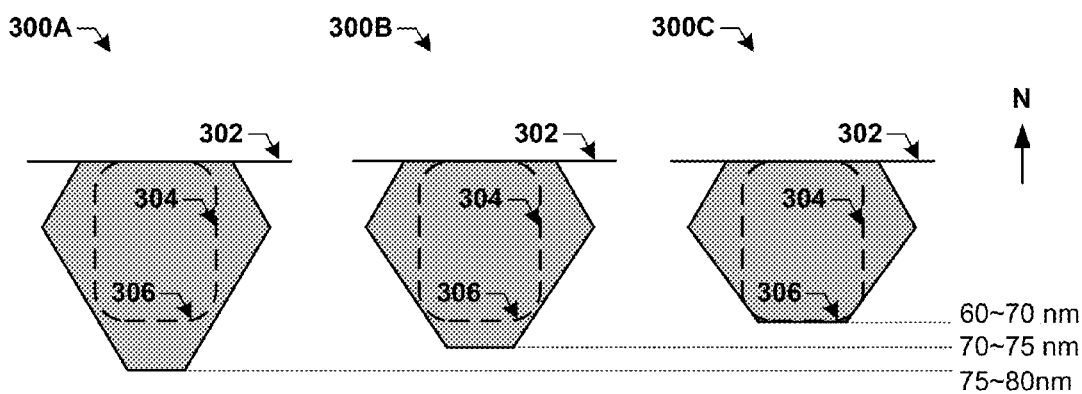
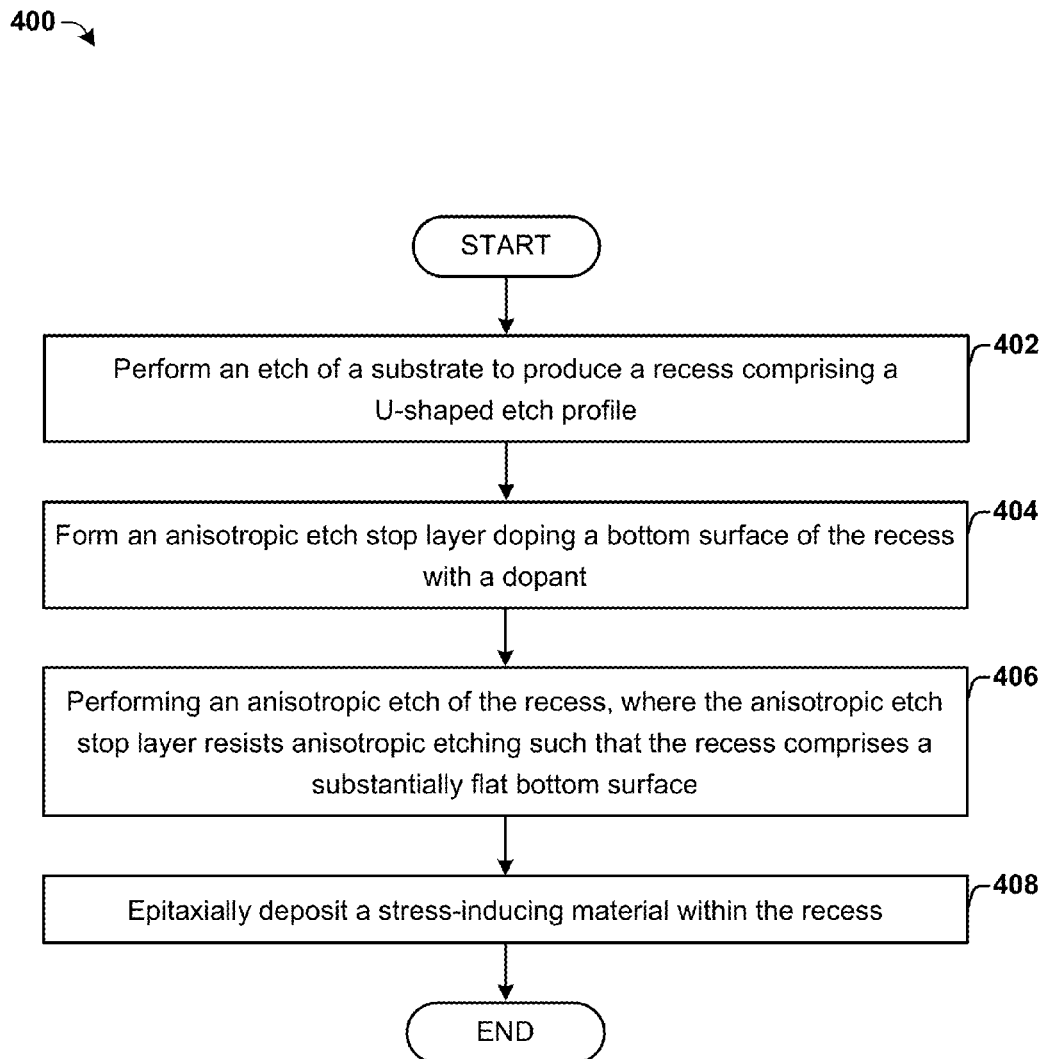


Fig. 3A

Fig. 3B

Fig. 3C

**Fig. 4**

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V-SHAPED SIGE RECESS VOLUME TRIM FOR IMPROVED DEVICE PERFORMANCE AND LAYOUT DEPENDENCE

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a Non-provisional application claiming priority to U.S. Provisional Patent Application Ser. No. 61/790,741 filed on Mar. 15, 2013 in the name of Chao-Hsuing Chen, which is entitled "V-SHAPED SIGE RECESS VOLUME TRIM FOR IMPROVED DEVICE PERFORMANCE AND LAYOUT DEPENDENCE" and which is hereby incorporated by reference in its entirety.

BACKGROUND

The following disclosure relates to semiconductor manufacturing methods. In particular, the following disclosure relates to method for forming a contact to a semiconductor device.

Strained-layer epitaxy to produce a strained channel with enhanced carrier mobility within a metal-oxide semiconductor field-effect transistor (MOSFET) is achieved through the formation of strained source and drain regions within the MOSFET.

BRIEF DESCRIPTION OF THE DRAWINGS

Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

FIG. 1 illustrates a cross-sectional view of an exemplary MOSFET containing strained source and drain epitaxial regions.

FIGS. 2A-2E illustrate some embodiments of recess formation.

FIGS. 3A-3C illustrate cross-sections of some embodiments of recess formation as a function of etch stop layer dopant concentration.

FIG. 4 illustrates some embodiments of a method of recess formation.

DETAILED DESCRIPTION

The following disclosure provides many different embodiments, or examples, for implementing different features of the subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

The description herein is made with reference to the drawings, wherein like reference numerals are generally utilized to

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refer to like elements throughout, and wherein the various structures are not necessarily drawn to scale. In the following description, for purposes of explanation, numerous specific details are set forth in order to facilitate understanding. It may be evident, however, to one of ordinary skill in the art, that one or more aspects described herein may be practiced with a lesser degree of these specific details. In other instances, known structures and devices are shown in block diagram form to facilitate understanding.

Strained source and drain regions are formed within a MOSFET through the formation of a recess within the source or drain region, and the deposition of a strain-inducing layer within the recess. A germanium-containing material such as a silicon germanium (SiGe) may be utilized for hole mobility enhancement of a p-channel MOSFET. SiGe deposited within the source or drain of the p-channel MOSFET will result in a uniaxial compressive strain within the channel due to the increased lattice constant of germanium (Ge) over silicon (Si). Similarly, a carbon-containing material such as silicon carbide (SiC) may be utilized for electron mobility enhancement of an n-channel MOSFET. SiC deposited within the source or drain of the n-channel MOSFET will result in a uniaxial tensile strain within the channel due to the decreased lattice constant of carbon (C) over Si. FIG. 1 illustrates a cross-sectional view of an exemplary MOSFET 100 formed on a Si or silicon-on-insulator (SOI) substrate 102 and containing a gate 104 residing beneath a hardmask layer 106 and isolated from source and drain regions by a first spacer 108A and a second spacer 108B, respectively. The source region comprises a first 110A comprising a diamond-shape or V-shape which has been filled with a stress-inducing material (e.g., SiGe, SiC, etc.) and a second recess 110B comprising an anisotropic etch profile (e.g., a diamond-shape or V-shape) which has been filled with the stress-inducing material.

For p-channel MOSFET channel mobility enhancement in advanced technology node development (i.e., Node-28 and below) a Ge concentration of greater than approximately 40% (e.g., $\text{Si}_{1-x}\text{Ge}_x$ where $x > 40\%$) may be utilized within the first or second recess 110A, 110B. First or second SiGe dislocations 112A, 112B within the first or second respective recess 110A, 110B formed at the SiGe/substrate interface can degrade device performance of the p-channel MOSFET 100, as well as distort the topologies of subsequent layers disposed above the stress-inducing material.

Accordingly, some embodiments of the present disclosure relates to a method and a device to achieve a strained channel. A volume of a source or drain recess is controlled by a performing an etch of a substrate to produce a recess. An anisotropic etch stop layer is then formed by doping a bottom surface of the recess with a boron-containing dopant, which distorts the crystalline structure of the bottom surface. An anisotropic etch of the recess is then performed. The anisotropic etch stop layer resists anisotropic etching such that the recess comprises a substantially flat bottom surface after the anisotropic etch. The source or drain recess is then filled with a stress-inducing material to produce a strained channel.

FIGS. 2A-2E illustrate some embodiments of recess formation. FIG. 2A illustrates a cross-sectional view of a device 200A formed on a substrate 202. In some embodiments, the substrate 202 comprises silicon (Si) or silicon-on-insulator (SOI), whereupon a gate 204 (e.g., poly-silicon, replacement metal, etc.) is disposed beneath a hardmask layer 206 (e.g., SiO_2 or other dielectric) and isolated from source and drain regions by a first spacer 208A (e.g., SiO_2 or other dielectric) and a second spacer 208B, respectively.

FIG. 2B illustrates a cross-sectional view of a device 200B comprising the device 200A where an etch of the substrate

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202 is performed to produce a first recess **210A** within the source region, where the first recess comprises a U-shaped etch profile. The etch of the substrate **202** also produces a second recess **210B** within the drain region also comprising a U-shaped etch profile. One or more etching processes may be used to recess the source and drain regions to produce the U-shaped etch profile.

In some embodiments, the etch used to recess the source and drain regions comprises an isotropic etch to produce an isotropic etch profile. In some embodiments, the etch comprises an anisotropic etch to produce an anisotropic etch profile. In some embodiments, the etch is performed in two or more steps that comprise a combination of and anisotropic elements. These elements can comprise dry process(es), such as a plasma etching process, wet etching process(es), reactive ion etching (RIE) processes, or a combination thereof. Such processes may include bombarding the substrate with ions (e.g., fluorocarbons, oxygen, chlorine, nitrogen, argon, helium, etc.) that dislodge portions of the material from the substrate **202**.

FIG. 2C illustrates a cross-sectional view of a device **200C** comprising the device **200B** where a first anisotropic etch stop layer **212A** is formed in the first recess **210A** by doping a bottom surface of the first recess **210A** with a dopant. Similarly, a second anisotropic etch stop layer **212B** is formed in the second recess **210B** by doping a bottom surface of the second recess **210B** with the dopant. For the embodiments of FIGS. 2A-2E, the dopant comprises a boron-containing material, and the doping is achieved through an ion implantation technique, performed at a zero angle with a normal vector **N** to a surface of the substrate **202**. An ionized boron implant dose of greater than approximately 2×10^{15} keV is demonstrated produce a boron concentration of greater than approximately 1×10^{20} atoms/cm³ within the first or second anisotropic etch stop layers **212A**, **212B**. The ion implantation technique is utilized at a zero angle with respect to **N** to achieve a distortion of the crystalline structure of the substrate **202** on a bottom surface of the first and second recess **210A**, **210B** such that sidewalls of the first and second recesses **210A**, **210B** are not distorted.

FIG. 2D illustrates a cross-sectional view of a device **200D** comprising the device **200C** where an anisotropic etch of the first and second recess **210A**, **210B** is performed. The first and second anisotropic etch stop layers **212A**, **212B** resists anisotropic etching such that the first and second recess **210A**, **210B** comprise substantially flat bottom surfaces. A boron impurity concentration of greater than approximately 1×10^{20} atoms/cm³ within the first or second anisotropic etch stop layers **212A**, **212B** is sufficient to prevent etching of the substantially flat bottom surfaces of the first and second recesses **210A**, **210B**.

The anisotropic etch of FIG. 2D comprises a wet etch. Some wet etchants etch crystalline materials at different rates depending upon which crystal face is exposed, resulting in an anisotropic etch. An etchant such as carbon tetrafluoride (CF₄), HF, tetramethylammonium hydroxide (TMAH), or combinations of thereof, may be used to perform the wet etch of the first and second recesses **210A**, **210B**. Other etchants such as potassium hydroxide (KOH) may be utilized for selective etching of silicon in the <100> direction. Ethylene diamine pyrocatechol (EDP) may also be utilized, and does not etch silicon dioxide as KOH does. TMAH demonstrates approximately twice the selectivity between the <100> and <111> directions in silicon over EDP. For the wet etch of FIG. 2D, the TMAH etchant demonstrates a high degree of selectivity between the (100) sidewalls of the first and second recesses **210A**, **210B** and the first and second anisotropic etch

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stop layers **212A**, **212B** due to the boron impurity concentration of greater than approximately 1×10^{20} atoms/cm³ within the first and second anisotropic etch stop layers **212A**, **212B**, and resulting distortion of the lattice structure of the substrate **202**.

The etch profiles of the first and second recesses **210A**, **210B** other than the bottom surfaces comprises a (100) crystal orientation after the anisotropic etch. For the embodiments of FIG. 2D the wet etch which utilizes TMAH as an etchant configured for preferred etch selectivity in the <100> direction. The boron-containing material distorts a crystal orientation of the bottom surface such that the TMAH etchant demonstrates non-preferred etch selectivity in a direction of the bottom surface.

In some embodiments, the anisotropic etch performed in FIG. 2B produces a first depth of the first and second recesses **210A**, **210B** of between approximately 60 nm and approximately 70 nm. A second depth after the isotropic etch of the first and second recesses **210A**, **210B** is approximately equal to a first depth due to the first and second isotropic etch stop layers **212A**, **212B**.

FIG. 2E illustrates a cross-sectional view of a device **200E** comprising the device **200D** where a first stress-inducing material **214A** is deposited in the first recess **210A** and a second stress-inducing material **214B** is deposited in the second recess **210B** through an epitaxial growth technique. In some embodiments, the epitaxial growth technique comprises chemical vapor deposition (CVD). Some derivative CVD processes further comprise low pressure CVD (LPCVD), atomic layer CVD (ALCVD), ultrahigh vacuum CVD (UHVCVD), reduced pressure CVD (RPCVD), or any combinations thereof. Molecular beam epitaxy (MBE) or metalorganic vapor phase epitaxy (MOVPE) may also be utilized for epitaxial growth. Another method, cyclic deposition-etch (CDE) epitaxy, comprises periodic exposure of the substrate **202** to the material through CVD or other epitaxial method, while periodically exposing the substrate **202** to no material, and so on, until a desired epitaxial layer is deposited. Throughout the CDE process, the substrate **202** is exposed to a continuous flow of one or more vapor etchants configured to selectively etch away amorphous portions of the epitaxial layer while leaving crystalline portions intact, facilitating high crystal quality for enhanced strain. Selective epitaxial growth (SEG) process may also be utilized, wherein simultaneous deposition and etch may be used to deposit the epitaxial layer.

The epitaxial layers of the first and second stress-inducing materials **214A**, **214B** within the first and second recesses **210A**, **210B** are configured to produce a strain within a channel region **216** of the device **200E** to increase the mobility of charge carriers within the channel region **216**, and thus increase the performance of the device **200E** under static biasing conditions. A germanium-containing material such as SiGe may be utilized for hole mobility enhancement of a p-channel MOSFET due to a uniaxial compressive strain within the channel region **216**. Likewise, a carbon-containing material such as SiC may be utilized for electron mobility enhancement of an n-channel MOSFET due to a uniaxial tensile strain within the channel region **216**. For the embodiments of FIG. 2E, the first and second stress-inducing materials **214A**, **214B** comprise silicon-germanium (SiGe) comprising a germanium composition of greater than 40%.

FIGS. 3A-3C illustrate cross-sections of some embodiments of recess formation as a function of etch stop layer dopant concentration. By varying the ionized boron implant energy in a range between approximately 2×10^{13} keV and approximately 2×10^{15} keV, the selectivity of the anisotropic

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etch may be enhanced between the bottom surface and side-walls of a respective recess. FIG. 3A illustrates a cross-section of a first anisotropic recess **300A** formed within a substrate comprising a surface **302**. The first anisotropic recess **300A** may be formed by multiple etch process comprising an isotropic dry etch (e.g., plasma etch) to form an isotropic recess **304** formed with a depth of between approximately 60 nm and approximately 70 nm, which is doped with ionized boron through an ion implant performed antiparallel to a normal vector **N** to the surface **302**, and with an implant energy of approximately 2E13 keV to form a first etch stop layer with a boron concentration of approximately 1e18 atoms/cm³. Subsequent to first etch stop layer formation, an anisotropic wet etch is performed with TMAH, which demonstrates selectivity between the sidewalls of the isotropic recess **304** and the first etch stop layer such that the sidewalls are etched anisotropically in the <100> direction, while the first etch stop layer resists etching, but is etched such that the first anisotropic recess **300A** resulting from the anisotropic etch has a depth of between approximately 75 nm and approximately 80 nm.

FIG. 3B illustrates a cross-section of a second anisotropic recess **300B**, which is formed in a manner similar to the first anisotropic recess **300A**, wherein only the implant energy of the boron implant is altered. Upon formation of the isotropic recess **304**, the bottom surface is doped with ionized boron with an implant energy of approximately 2E14 keV to form a second etch stop layer with a boron concentration of approximately 1e19 atoms/cm³. The subsequent anisotropic wet etch performed with TMAH demonstrates increased selectivity between the sidewalls of the isotropic recess **304** and the second etch stop layer due to the increased boron concentration, such that the anisotropic etch results in a depth of between approximately 70 nm and approximately 75 nm. FIG. 3C illustrates a cross-section of a third anisotropic recess **300C** formed in the same manner as the first and second anisotropic recesses **300A**, **300B**, wherein only the implant energy of the boron implant is altered to approximately 2E15 keV, resulting in a boron concentration of greater than approximately 1e20 atoms/cm³ within a resulting third etch stop layer at the bottom surface **306**. The increased selectivity between the sidewalls and the bottom surface **306** results in essentially no etching of the bottom surface due to the third etch stop layer, such that the third anisotropic recess **300C** comprises a substantially flat bottom surface **306**, and further comprises a depth of between approximately 60 nm and approximately 70 nm, which is the original depth of the isotropic recess **304**. The third anisotropic recess **300C** may then be filled with a stress-inducing material. In some embodiments, the stress-inducing material comprises SiGe comprising a germanium composition of greater than 40% for a p-channel MOSFET. In some embodiments, the stress-inducing material comprises a carbon-containing material such as SiC for an n-channel MOSFET.

FIG. 4 illustrates some embodiments of a method **400** of recess formation. While the method **400** is illustrated and described as a series of acts or events, it will be appreciated that the illustrated ordering of such acts or events are not to be interpreted in a limiting sense. For example, some acts may occur in different orders or concurrently with other acts or events apart from those illustrated or described herein. In addition, not all illustrated acts may be required to implement one or more aspects or embodiments of the description herein. Further, one or more of the acts depicted herein may be carried out in one or more separate acts or phases.

At **402** an etch of a substrate is performed to produce a recess comprising a U-shaped etch profile. The substrate may

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comprise a silicon (Si) or silicon-on-insulator (SOI) substrate. In some embodiments, the etch comprises a dry etch, wet etch, plasma etch, RIE etch, or a combination thereof.

At **404** an anisotropic etch stop layer is formed through an ion implantation technique by implanting a dopant comprising a boron-containing material on a bottom surface of the recess. The implant distorts a crystal orientation of the bottom surface of the recess such that an anisotropic etchant will demonstrate a non-preferred etch selectivity in a direction of the bottom surface. The implantation is performed through an ion implantation technique at a zero angle with a normal vector to the substrate surface and with an implant energy of greater than approximately 1e15 keV produce a boron impurity concentration of greater than approximately 1e20 atoms/cm³ within the bottom surface.

At **406** an anisotropic etch of the recess is performed, wherein the anisotropic etch stop layer resists anisotropic etching such that the recess comprises a substantially flat bottom surface. In some embodiments, the anisotropic etch comprises a wet etch which utilizes TMAH as an etchant configured for preferred etch selectivity in the <100> direction of the Si or SOI substrate. The resultant etch profile of the recess other than the bottom surface comprises a (100) crystal orientation after the anisotropic etch. For a large enough boron impurity concentration a second depth of the recess after the anisotropic etch is approximately equal to a first depth of the recess after the isotropic etch, because the bottom surface is not etched.

At **408** a stress-inducing material is epitaxially deposited within the recess. The stress-inducing material may comprise SiGe comprising a germanium composition of greater than 40%, or a carbon-containing material such as SiC.

It will also be appreciated that equivalent alterations or modifications may occur to one of ordinary skill in the art based upon a reading or understanding of the specification and annexed drawings. The disclosure herein includes all such modifications and alterations and is generally not intended to be limited thereby. In addition, while a particular feature or aspect may have been disclosed with respect to only one of several implementations, such feature or aspect may be combined with one or more other features or aspects of other implementations as may be desired. Furthermore, to the extent that the terms “includes”, “having”, “has”, “with”, or variants thereof are used herein; such terms are intended to be inclusive in meaning—like “comprising.” Also, “exemplary” is merely meant to mean an example, rather than the best. It is also to be appreciated that features, layers or elements depicted herein are illustrated with particular dimensions or orientations relative to one another for purposes of simplicity and ease of understanding, and that the actual dimensions or orientations may differ substantially from that illustrated herein.

Therefore, some embodiments of the present disclosure relates to a method and a device to achieve a strained channel. A volume of a source or drain recess is controlled by a performing an etch of a substrate to produce a recess. An anisotropic etch stop layer is then formed by doping a bottom surface of the recess with a boron-containing dopant, which distorts the crystalline structure of the bottom surface. An anisotropic etch of the recess is then performed. The anisotropic etch stop layer resists anisotropic etching such that the recess comprises a substantially flat bottom surface after the anisotropic etch. The source or drain recess is then filled with a stress-inducing material to produce a strained channel.

In some embodiments the present disclosure relates to a method of recess formation, comprising performing an etch of a substrate to produce a recess comprising a U-shaped etch

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profile. The method further comprises forming an anisotropic etch stop layer by doping a bottom surface of the recess with a dopant. The method further comprises performing an anisotropic etch of the recess, wherein the anisotropic etch stop layer resists anisotropic etching such that the etch profile comprises a substantially flat bottom surface after the anisotropic etch. The method further comprises epitaxially depositing a stress-inducing material within the recess.

In some embodiments the present disclosure relates to a method of recess formation, comprising performing an etch of a silicon (Si) or silicon-on-insulator (SOI) substrate to produce a recess comprising a U-shaped etch profile. The method further comprises forming an anisotropic etch stop layer by implanting a dopant comprising a boron-containing material on a bottom surface of the recess. The method further comprises performing an anisotropic etch of the recess, wherein the anisotropic etch stop layer resists anisotropic etching such that the recess comprises a substantially flat bottom surface. A second depth of the recess after the anisotropic etch is approximately equal to a first depth of the recess after the etch. The method further comprises epitaxially depositing a stress-inducing material within the recess;

In some embodiments the present disclosure relates to a device, comprising source and drain regions comprising a stress-inducing material which are separated by a gate, having a boron concentration of greater than approximately $1e20$ atoms/cm³ below the stress-inducing material in the source and drain regions.

What is claimed is:

1. A method of recess formation, comprising:
 - performing an etch of a substrate to produce a recess comprising a U-shaped etch profile having curved sidewalls, wherein the U-shaped etch profile has a largest width at an opening along a top surface of the substrate;
 - forming an anisotropic etch stop layer by doping a bottom surface of the recess with a dopant;
 - performing an anisotropic etch of the recess to form a source/drain recess, wherein the anisotropic etch stop layer resists anisotropic etching such that the etch profile of the source/drain recess comprises a substantially flat bottom surface after the anisotropic etch; and
 - epitaxially depositing a stress-inducing material within the source/drain recess onto the anisotropic etch stop layer.
2. The method of claim 1, wherein of the substrate comprises silicon (Si) or silicon-on-insulator (SOI), and wherein surfaces of the recess other than the bottom surface comprises a (100) crystal orientation after the anisotropic etch.
3. The method of claim 2, wherein the anisotropic etch comprises a wet etch which utilizes Tetramethylammonium hydroxide (TMAH) as an etchant configured for preferred etch selectivity in a <100> direction.
4. The method of claim 3, wherein doping the bottom surface comprises implanting the dopant such that the TMAH etchant demonstrates non-preferred etch selectivity in a direction of the bottom surface.
5. The method of claim 4, wherein the dopant comprises a boron-containing material.
6. The method of claim 5, wherein doping the bottom surface of the recess is performed by implantation at a zero angle with a normal vector to a surface of the substrate and with a boron implant energy of greater than approximately $1e15$ keV to produce a boron impurity concentration of greater than approximately $1e20$ atoms/cm³ within the substantially flat bottom surface.
7. The method of claim 1, wherein a second depth of the source/drain recess after the anisotropic etch is approximately equal to a first depth of the recess after the etch.

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8. The method of claim 1, wherein the etch profile is symmetric about a line bisecting the etch profile.

9. The method of claim 1, wherein the etch profile comprises opposing sidewalls that are angled away from the anisotropic etch stop layer.

10. The method of claim 1, wherein the anisotropic etch removes a part of the anisotropic etch stop layer, so that the source/drain recess has a greater depth than the recess.

11. The method of claim 10, wherein the source/drain recess has angled sidewalls that vertically extend into the anisotropic etch stop layer.

12. The method of claim 1, wherein the source/drain recess having planar angled sidewalls that directly contact sidewalls of the anisotropic etch stop layer.

13. A method of recess formation, comprising:

performing an etch of a substrate to produce a recess comprising a U-shaped etch profile;

forming an anisotropic etch stop layer by implanting a dopant comprising a boron-containing material on a bottom surface of the recess;

performing an anisotropic etch of the recess to form a source/drain recess comprising a substantially flat bottom surface, wherein the source/drain recess is symmetric about a vertical line bisecting the anisotropic etch stop layer arranged along the substantially flat bottom surface of the source/drain recess and wherein the source/drain recess having planar angled sidewalls that directly contact both sidewalls of the anisotropic etch stop layer symmetrically; and

epitaxially depositing a stress-inducing material within the source/drain recess.

14. The method of claim 13, wherein:

the etch comprises a dry etch;

the anisotropic etch comprises a wet etch which utilizes Tetramethylammonium hydroxide (TMAH) as an etchant configured for preferred etch selectivity in a <100> direction; and

the implant distorts a crystal orientation of the bottom surface such that the TMAH etchant demonstrates non-preferred etch selectivity in a direction of the bottom surface.

15. The method of claim 13, wherein the implanting is performed at a zero angle with a normal vector to a surface of the substrate and with a boron implant energy of greater than approximately $1e15$ keV to produce a boron impurity concentration of greater than approximately $1e20$ atoms/cm³ within the substantially flat bottom surface.

16. The method of claim 13, wherein the stress-inducing material comprises silicon-germanium (SiGe) comprising a germanium composition of greater than 40%, or a carbon-containing material.

17. A device, comprising:

a source region and a drain region arranged within a substrate and comprising a stress-inducing material;

an etch stop layer arranged along flat lower surfaces of the source region and the drain region, wherein the source region is symmetric about a vertical line bisecting the etch stop layer arranged along a flat lower surface of the source region and wherein the source region and the drain region have planar angled sidewalls that directly contact both sidewalls of the etch stop layer symmetrically;

a gate structure arranged over the substrate at a location that is laterally between the source and drain regions; and

wherein the etch stop layer has a boron concentration of greater than approximately 1×10^{20} atoms/cm³ below the stress-inducing material in the source and drain regions.

18. The device of claim **17**, wherein the stress-inducing material comprises silicon-germanium (SiGe). 5

19. The device of claim **17**, wherein the stress-inducing material comprises a germanium composition of greater than 40%.

20. The device of claim **17**, wherein the stress-inducing material comprises carbon. 10

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